REMARKS/ARGUMENTS

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

Claims 1-21 are pending in the present application. With this amendment, claims 5-6, 12-13, and 19-20 have been canceled; claims 1-4, 7-11, 14-18, and 21 have been amended; and claims 22-24 were added. Reconsideration of the claims is respectfully requested.

I. Examiner Interview

Applicant appreciates the courtesies extended by the Examiner in the interview that was conducted on February 7, 2007. Applicant's claims were discussed. No agreement was reached.

II. Claim Objections

The Examiner noted several informalities in the claims. These informalities have been corrected. Therefore, these objections should be withdrawn.

III. 35 U.S.C. § 101

The Examiner has rejected claims 15-21 under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

The Examiner stated that "the claimed 'computer readable medium' as described in the specification page(s) 20, lines 2-5, includes, among other examples, transmission-type media, such as digital and analog communication links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmission, which is nonstatutory. As such, the claim is not limited to statutory subject matter and is therefore nonstatutory."

Applicant has amended the specification to delete the language regarding "transmission-type media". Therefore, this rejection is believed to be overcome by the amendments to the specification and should be withdrawn.

IV. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1, 2, 8, 9, 15 and 16 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 7,017,074 issued to *Okin*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicant has amended claims 1, 8, and 15. Claims 1, 8, and 15 recite similar features. Claim 1 recites: responsive to detecting a failed processor in a first set of processors on a first multi-chip module, determining whether a first spare processor from said first set of processors is available to replace said failed processor; in response to determining that said first spare processor is available, assigning the first spare processor to replace the failed processor; in response to determining that said first spare processor is unavailable, determining whether a second spare processor from a second set of processors on a second multi-chip module is available to replace said failed processor; in response to determining that said second spare processor is available, assigning the second spare processor to replace said failed processor; and simultaneously utilizing said first multi-chip module to execute code for a first operating system and utilizing said second multi-chip module to execute code for a second operating system.

Some examples of support for these amendments can be found in the specification on page 6, lines 22-26; page 7, lines 6-23; page 10, lines 27-30; and page 14, lines 14-30.

Okin teaches a chip that includes multiple processors formed on a die. If one of the processors fails, a saved state for that processor is transferred to a functioning processor.

Okin does not anticipate Applicant's amended independent claims because *Okin* does not teach in response to determining that said first spare processor is unavailable, determining whether a second spare processor from a second set of processors on a second multi-chip module is available to replace said failed processor; in response to determining that said second spare processor is available, assigning the second spare processor to replace said failed processor; and simultaneously utilizing said first multi-chip module to execute code for a first operating system and utilizing said second multi-chip module to execute code for a second operating system.

Therefore, the rejection of claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 102(e) has been overcome.

The Examiner has rejected claims 5, 12 and 19 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,485,604, issued to *Miyoshi*. Applicant has canceled claims 5, 12, and 19. Therefore, this rejection should be withdrawn.

V. 35 U.S.C. § 103(a), Obviousness

The Examiner has rejected claims 1-3, 6-10, 13-17, 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over *Miyoshi* in view of *Okin*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Miyoshi teaches a fault tolerant computer system that includes multiple CPUs. One of these CPUs is a master module. The other CPUs act as checker modules. If the master module fails, one of the checker CPUs becomes the master module.

Miyoshi does not teach two multi-chip modules, each with a set of processors. The CPU, also referred to as a central processor module, taught by *Miyoshi* is not a multi-chip module that includes a set of processors.

Neither *Miyoshi* nor *Okin* teaches simultaneously utilizing said first multi-chip module to execute code from a first operating system and utilizing said second multi-chip module to execute code from a second operating system. *Okin* teaches one chip, so *Okin* cannot teach utilizing said first multi-chip module to execute code from a first operating system and utilizing said second multi-chip module to execute code from a second operating system. *Miyoshi* teaches one CPU acting as a master module. *Miyoshi* teaches a master CPU and checker CPUs. *Miyoshi* does not teach the master CPU executing code from a first operating system and one of the checker CPUs executing code from a second operating system.

The combination of *Miyoshi* and *Okin* does not render Applicant's claims obvious. Therefore, the rejection of claims 1-3, 6-10, 13-17, 20 and 21 under 35 U.S.C. § 103(a) has been overcome.

The Examiner has rejected claims 4, 11 and 18 under 35 U.S.C. § 103(a) as being unpatentable over *Okin* in view of U.S. Patent 5,867,658, issued to *Lee* and U.S. Patent 5,802,365, issued to *Kathail*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

These claims describe wherein the first spare processor and the second spare processor are each marked by an open firmware.

The combination of *Okin*, *Lee*, and *Kathail* does not render Applicant's claims obvious because the combination does not teach responsive to detecting a failed processor in a first set of processors on a first multi-chip module, determining whether a first spare processor from said first set of processors is available to replace said failed processor; in response to determining that said first spare processor is available, assigning the first spare processor to replace the failed processor; in response to determining that said first spare processor is unavailable, determining whether a second spare processor from a second set of processors on a second multi-chip module is available to replace said failed processor; in response to determining that said second spare processor is available, assigning the second processor to replace said failed processor; and simultaneously utilizing said first multi-chip module to execute code from a first operating

system and utilizing said second multi-chip module to execute code from a second operating system in combination with wherein the first spare processor and the second spare processor are each marked by an open firmware.

The Examiner has rejected claims 4, 11 and 18 under 35 U.S.C. § 103(a) as being unpatentable over *Miyoshi* in view of *Okin* and further in view of *Lee* and *Kathail*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

These claims describe wherein the first spare processor and the second spare processor are each marked by an open firmware.

The combination of *Miyoshi*, *Okin*, *Lee*, and *Kathail* does not render Applicant's claims obvious because the combination does not teach responsive to detecting a failed processor in a first set of processors on a first multi-chip module, determining whether a first spare processor from said first set of processors is available to replace said failed processor; in response to determining that said first spare processor is available, assigning the first spare processor to replace the failed processor; in response to determining that said first spare processor is unavailable, determining whether a second spare processor from a second set of processors on a second multi-chip module is available to replace said failed processor; in response to determining that said second spare processor is available, assigning the second processor to replace said failed processor; and simultaneously utilizing said first multi-chip module to execute code from a first operating system and utilizing said second multi-chip module to execute code from a second operating system in combination with wherein the first spare processor and the second spare processor are each marked by an open firmware.

Therefore, the rejection of claims 4, 11 and 18 under 35 U.S.C. § 103(a) has been overcome.

VI. Conclusion

It is respectfully urged that the subject application is patentable over the cited prior art and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: February 14, 2007

Respectfully submitted,

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